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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael R. Krause et al.	Examiner:	George C. Neurauter
Serial No.:	09/980,920	Group Art Unit:	2143
Filed:	April 11, 2002	Docket No.:	10002166-2
Title:	MEMORY MANAGEMENT IN DISTRIBUTED COMPUTER SYSTEM		

CERTIFICATE OF TRANSMISSION

Commissioner for Patents
P.O. Box 1450
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Name: Patrick G. Billig (Reg. No. 38,080)

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PATENT APPLICATION

ATTORNEY DOCKET NO. 10002166-2

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Michael R. Krause et al.

Confirmation No.: 3383

Application No.: 09/980,920

Examiner: George C. Neurauter

Filing Date: April 11, 2002

Group Art Unit: 2143

Title: MEMORY MANAGEMENT IN DISTRIBUTED COMPUTER SYSTEM

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on April 27, 2007.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Date of facsimile: June 27, 2007
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Respectfully submitted,
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By /Patrick G. Billig/
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Rev 10/05 (ApBrief)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Michael R. Krause et al.	Examiner: George C. Neurauter
Serial No.:	09/980,920	Group Art Unit: 2143
Filed:	April 11, 2002	Docket No.: 10002166-2
Title:	MEMORY MANAGEMENT IN DISTRIBUTED COMPUTER SYSTEM	

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed on April 27, 2007, appealing the final rejection of claims 1-34of the above-identified application as set forth in the Final Office Action mailed February 27, 2007.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $500.00 for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. §41.20(b)(2). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1-34.

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Appeal Brief to the Board of Patent Appeals and Interferences
Appellant: Michael R. Krause et al.
Serial No.: 09/980,920
Filed: April 11, 2002
Docket No.: 10002166-2
Title: MEMORY MANAGEMENT IN DISTRIBUTED COMPUTER SYSTEM

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REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed February 27, 2007, claims 1-34 were finally rejected. Claims 1-34 are pending in the application, and are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been entered subsequent to the Final Office Action mailed February 27, 2007.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The subject matter of the independent claims involved in the Appeal is related to managing memory in a distributed computer system. The Summary is set forth as exemplary embodiments corresponding to the language of independent claims 1 and 19. Discussions about elements of claims 1 and 19 can be found at least at the cited locations in the specification and drawings.

One aspect of the present invention, as claimed in independent claim 1, provides a method of managing memory in a distributed computer system (700). The method comprises binding a remote key (746) to a first address (744) representing a contiguous memory address range (720) accessible by a first consumer process (718) stored in a first memory (706) at a first host processor endnode (702) including a first processor (704) and the first memory. The method comprises sending the bound remote key and first address from the first host

processor endnode to a second host processor endnode (703) on a communication fabric (722) via a first networking interface controller (NIC) (714) in the first host processor endnode and a second NIC (734) in the second host processor endnode. The second host processor endnode includes a second processor (724) and a second memory (726). The method comprises performing a remote direct memory access operation from the second host processor endnode with a second consumer process (738) stored in the second memory to access the contiguous memory address range including sending the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric via the second NIC and the first NIC. *See specification at page 34, line 26 through page 38, line 30 and Figure 18.*

One aspect of the present invention, as claimed in independent claim 19, provides a distributed computer system (700) comprising a communication fabric (722). The distributed computer system comprises a first host processor endnode (702) including a first processor (704), a first memory (706) configured to store a first consumer process (718) which binds a remote key (746) to a first address (744) representing a contiguous memory address range (720) accessible by the consumer process, and a first network interface controller (NIC) (714) sending the bound remote key and first address from the first host processor endnode on the communication fabric. The distributed computer system comprises a second host processor (703) including a second processor (724), a second (NIC) (734) receiving the bound remote key and first address from the first host processor endnode via the communication fabric and a second memory (726) configured to store a second consumer process (738) performing a remote direct memory access operation from the second host processor endnode to access the contiguous memory address range including sending, via the second NIC, the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric. *See specification at page 34, line 26 through page 38, line 30 and Figure 18.*

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 1, 2, 6, 7, 9-13, 16, 17, 19, 20, 23-29, 32, and 33 stand rejected under 35 U.S.C. §102(e) as anticipated by the Futral et al. U.S. Patent No. 5,991,797.

II. Claims 3-5, 8, 21, 22, and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the Futral et al. U.S. Patent No. 5,991,797 in view of the Regnier et al. U.S. Patent No. 6,647,423.

III. Claims 14, 15, 18, 30, 31, and 34 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the Futral et al. U.S. Patent No. 5,991,797 in view of the Forin et al. U.S. Patent No. 6,360,220.

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ARGUMENT

I. The Applicable Law

To anticipate a claim under 35 U.S.C. 102, a reference must teach every element of the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) ("A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference").

With regard to a 35 U.S.C. § 103 obviousness rejection: "Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case." M.P.E.P. 2141 (emphasis in the original). The Examiner bears the burden under 35 U.S.C. § 103 in establishing a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *In re Fine* at 1074. Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375, 379 (Fed. Cir. 1986). Third, the reference or combined references must teach or suggest all of the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (C.C.P.A. 1974).

The court in *Fine* stated:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." And "teachings of references can be combined *only* if there is some suggestion or incentive to do so."

In re Fine, 5 USPQ2d at 1599 (citations omitted).

There must be some teaching somewhere that provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem that it addresses. *In re Nilssen*, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988); *In re Wood*, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (C.C.P.A. 1979). In

particular, "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based upon Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142 (emphasis added).

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985). Furthermore, claims must be interpreted in light of the specification, claim language, other claims, and prosecution history. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1568, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987), *cert. denied*, 481 U.S. 1052 (1987). At the same time, a prior patent cited as a § 103 reference must be considered in its entirety, "*i.e.* as a *whole*, including portions that lead away from the invention." *Id.* That is, the Examiner must recognize and consider not only the similarities, but also the critical differences between the claimed invention and the prior art as one of the factual inquiries pertinent to any obviousness inquiry under 35 U.S.C. § 103. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990) (emphasis added). Finally, the Examiner must avoid hindsight. *Id.*

With regard for the test for obviousness under § 103, a statement that modifications of the prior art to meet the claimed invention would have been " 'well within the ordinary skill of the art at the time the claimed invention was made' " because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993); M.P.E.P. § 2143.01 (emphasis in the original).

In conclusion, an Appellant is entitled to a patent grant if any one of the elements of a prima facie case of obviousness is not established. The Federal Circuit has endorsed this view in stating: "If examination at the initial stage does not produce a prima facie case of unpatentability, then without more the Appellant is entitled to grant of the patent." In re Oetiker, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1448 (Fed. Cir. 1992).

II. Rejection of claims 1, 2, 6, 7, 9-13, 16, 17, 19, 20, 23-29, 32, and 33 under 35 U.S.C. §102(e) as anticipated by the Futral et al. U.S. Patent No. 5,991,797.

Independent claim 1 claims a method of managing memory in a distributed computer system and independent claim 19 claims a distributed computer system. Independent claim 1 and independent claim 19 include limitations related to binding a remote key to a first address representing a contiguous memory address range accessible by a first consumer process stored in a first memory at a first host processor endnode including a first processor and the first memory; sending the bound remote key and first address from the first host processor endnode to a second host processor endnode on a communication fabric via a first network interface controller (NIC) in the first host processor endnode and a second NIC in the second host processor endnode, wherein the second host processor endnode includes a second processor and a second memory; and performing a remote direct memory access operation from the second host processor endnode with a second consumer process stored in the second memory to access the contiguous memory address range including sending the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric via the second NIC and the first NIC. The Futral et al. patent does not teach or suggest all of these limitations.

The Futral et al. patent teaches a method for directing transfer of input/output (I/O) of an I/O device to other processing units in a computer system including first and second processing units and an I/O unit coupled to an interconnect fabric. The second processing unit controls access to the I/O unit, which is coupled to an I/O device. Memory fragments of the first processing unit are registered with the interconnect fabric to get memory handles for the memory fragments. A list is created having an identifier of the first processing unit, the memory handles, and virtual addresses and links of memory fragments. The list is sent from the first processing unit to the second processing unit. The list is sent from the second processing unit to the I/O unit. The identifier of the first processing unit is examined and a communications connection from the I/O unit to the first processing unit is determined. I/O data is transferred over the communication connection between and I/O unit and memory referenced by the memory handles and virtual addresses. The method supports peer-to-peer operation where a number of different I/O units, each with its own physical memory addressing domain, require access to the same I/O device. In the embodiment specifically

described at column 5 referenced by the Examiner, the combination of a platform identifier, a memory handle for registered memory, and a virtual address uniquely identifies memory located anywhere in a clustered computer system.

Thus, the Futral et al. patent does not teach or suggest limitations of independent claim 1 and independent claim 19 related to performing **a remote direct memory access operation from a second host processor endnode with a second consumer process stored in a second memory of the second host processor endnode** to access a contiguous memory address range accessible by a first consumer process stored in a first memory at a first host processor endnode, wherein the remote direct memory access operation includes sending the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric via the second NIC and the first NIC. Instead, the Futral et al. patent teaches a second host system directing **an I/O device to transfer data between** a requesting application program's buffers on **a first host system and an I/O unit** coupled to the I/O device **without the need to pass through the second host system**, where the second host system retains control of the I/O request.

In the non-final Office Action mailed July 7, 2006, at page 3 in the Response to Arguments, the Examiner equates "I/O device" or "I/O unit" or "host" as interchangeable terms. As presented in the Remarks of the Amendment and Response filed December 7, 2006 in response to the July 7, 2006 non-final Office Action, these terms and their definitions in the method and computer system disclosed in the Futral et al. patent are all distinctly defined as summarized in the above remarks. Accordingly, a host processor endnode in independent claims 1 and 19 and as clearly defined in the current specification is in no way equivalent to an I/O device or I/O unit. This distinction is clear from both the current specification and claims and the disclosed method and computer system of the Futral et al. patent.

In the Final Office mailed February 27, 2007, at pages 2-3 in the Response to Arguments, the Examiner disagrees with the Remarks filed by Applicant in the Amendment and Response filed December 7, 2006. The Examiner specifically refers to the Futral et al. patent at column 4, lines 45-50 which states, "host systems and I/O units are generically called units. A unit may have multiple SAN NICs installed. SAN NICs attach a unit to the SAN Fabric. The SAN NIC provides connections to other units that are external to the unit."

This section of the Futral et al. patent merely states there is a generic term for host systems and I/O units, but the host system is one specific type of unit and the I/O unit is another specific type of unit. Examples of the clear distinction between the teams host system, I/O unit, and I/O device are illustrated, for example, in Figure 1 of the Futral et al. patent where host system 10 and host system 16 are illustrated along with I/O unit 14 and I/O device 12 and also, for example, in Figure 2, where cluster host systems 20, 22, and 24 are illustrated along with I/O units 30, 32, and 34 along with corresponding I/O devices. Thus, as indicated above, host systems, I/O units, and I/O devices are separate and distinctly described and illustrated in detail in the Futral et al. patent. Furthermore, a host processor endnode as recited in independent claims 1 and 19 is in no way equivalent to an I/O device or I/O unit.

In addition, the Examiner states in the non-final Office Action mailed July 7, 2006, at page 3 in the Response to Arguments that the "SAN NIC" inherently contains a processor and memory. Both independent claim 1 and independent claim 19 specifically define operations performed by a first network interface controller (NIC) in the first host processor endnode and a second NIC in the second host processor endnode. The Futral et al. patent also specifically defines functions of the SAN NICs in its described computer system. Thus, as clearly defined in independent claims 1 and 19, the first processor and the first memory in the first host processor endnode are separate and distinct from the NIC in the first processor endnode and the second processor and the second memory in the second host processor endnode are separate and distinct from the second NIC in the second host processor endnode.

In view of the above, the Futral et al. patent does not teach or suggest the method of independent claim 1 or the distributed computer system of independent claim 19. Therefore, the Futral et al. patent does not anticipate independent claims 1 and 19.

Furthermore, dependent claims 2, 6, 7, 9-13, 16, and 17 further define patentable distinct independent claim 1 and dependent claims 20, 23-29, 32, and 33 further define patentably distinct independent claim 19. Therefore, these dependent claims are also not anticipated by the Futral et al. patent.

Therefore, Appellant respectfully requests reversal of the rejection of claims 1, 2, 6, 7, 9-13, 16, 17, 19, 20, 23-29, 32, and under 35 U.S.C. § 102 and allowance of these claims.

III. Rejection of claims 3-5, 8, 21, 22, and 25 under 35 U.S.C. §103(a) as being unpatentable over the Futral et al. U.S. Patent No. 5,991,797 in view of the Regnier et al. U.S. Patent No. 6,647,423.

In view of the above, the Futral et al. patent does not teach or suggest the method of independent claim 1 or the distributed computer system of independent claim 19. The Regnier et al. patent does not teach or suggest the limitations of independent claims 1 and 19 not taught in the Futral et al. patent. Therefore, the third criteria of a *prima facie* case of obviousness is not satisfied as the combination of the Futral et al. patent and the Regnier et al. patent does not teach or suggest all of the limitations of independent claims 1 and 19. Dependent claims 3-5, and 8 further define patentable distinct independent claim 1 and dependent claims 21, 22, and 25 further define patentably distinct independent claim 19. Therefore, these dependent claims are also not rendered obvious by the combination of the Futral et al. patent and the Regnier et al. patent.

Therefore, Appellant respectfully requests reversal of the rejection of claims 3-5, 8, 21, 22, and 25 under 35 U.S.C. § 103(a) and allowance of these claims.

IV. Rejection of claims 14, 15, 18, 30, 31, and 34 under 35 U.S.C. §103(a) as being unpatentable over the the Futral et al. U.S. Patent No. 5,991,797 in view of the Forin et al. U.S. Patent No. 6,360,220.

In view of the above, the Futral et al. patent does not teach or suggest the method of independent claim 1 or the distributed computer system of independent claim 19. The Forin et al. patent does not teach or suggest the limitations of independent claims 1 and 19 not taught in the Futral et al. patent. Therefore, the third criteria of a *prima facie* case of obviousness is not satisfied as the combination of the Futral et al. patent and the Forin et al. patent does not teach or suggest all of the limitations of independent claims 1 and 19. Dependent claims 14, 15, and 18 further define patentable distinct independent claim 1 and dependent claims 30, 31, and 34 further define patentably distinct independent claim 19. Therefore, these dependent claims are also not rendered obvious by the combination of the Futral et al. patent and the Forin et al. patent.

Therefore, Appellant respectfully requests reversal of the rejection of claims 14, 15, 18, 30, 31, and 34 under 35 U.S.C. § 103(a) and allowance of these claims.

CONCLUSION

For the above reasons, Appellant respectfully submits that the cited references neither anticipate nor render obvious claims of the pending Application. The pending claims distinguish over the cited references, and therefore, Appellant respectfully submits that the rejections must be withdrawn, and respectfully request the Examiner be reversed and claims 1-34 be allowed.

Any inquiry regarding this Appeal Brief should be directed to either Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005 or Kevin Hart at Telephone No. (970) 898-7057, Facsimile No. (970) 898-7247. In addition, all correspondence should continue to be directed to the following address:

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Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously Presented) A method of managing memory in a distributed computer system, the method comprising:

binding a remote key to a first address representing a contiguous memory address range accessible by a first consumer process stored in a first memory at a first host processor endnode including a first processor and the first memory;

sending the bound remote key and first address from the first host processor endnode to a second host processor endnode on a communication fabric via a first networking interface controller (NIC) in the first host processor endnode and a second NIC in the second host processor endnode, wherein the second host processor endnode includes a second processor and a second memory; and

performing a remote direct memory access operation from the second host processor endnode with a second consumer process stored in the second memory to access the contiguous memory address range including sending the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric via the second NIC and the first NIC.

2. (Previously Presented) The method of claim 1 further comprising:

controlling local memory access protection in the first host processor endnode with a virtual memory manager in an operating system kernel process stored in the first memory.

3. (Previously Presented) The method of claim 1 further comprising:

comparing the bound remote key and the corresponding first address supplied by the second host processor endnode to the bound remote key and corresponding first address in the first host processor endnode.

4. (Previously Presented) The method of claim 3 wherein if the bound remote key and corresponding first address supplied by the second host processor endnode do not match the bound remote key and first address in the first host processor endnode, the second host processor endnode is not granted access to the contiguous memory address range.

5. (Previously Presented) The method of claim 3 wherein if the contiguous memory address range represented by the first address bound to the remote key supplied by the second host processor endnode is invalid, the second host processor endnode is not granted access to the contiguous memory address range.

6. (Previously Presented) The method of claim 1 wherein the first address is an effective address pointing to an address space in the first memory accessible by the first consumer process.

7. (Previously Presented) The method of claim 6 wherein the effective address points to a virtual address space.

8. (Previously Presented) The method of claim 7 further comprising:

comparing the bound remote key and the corresponding first virtual address supplied by the second host processor endnode to the bound remote key and corresponding first virtual address in the first host processor endnode; and

handling a page fault condition in the first host processor endnode caused by the first virtual address bound to the remote key supplied by the second host processor endnode not being previously mapped by an operating system of the first host processor endnode.

9. (Previously Presented) The method of claim 1 wherein the first consumer process is a user process.

10. (Previously Presented) The method of claim 1 wherein the first consumer process is a kernel process.

11. (Previously Presented) The method of claim 1 wherein the first address is a virtual address accessible by the first consumer process which is a consumer kernel process.

12. (Previously Presented) The method of claim 1 wherein the binding includes associating the first address to the remote key with a consumer process employing a bind remote key verb.

13. (Previously Presented) The method of claim 1 further comprising:

obtaining at least one remote key with a consumer process employing an allocate remote key verb.

14. (Previously Presented) The method of claim 1 further comprising:

unbinding the remote key from the first address with a consumer process employing an unbind remote key verb.

15. (Previously Presented) The method of claim 13 further comprising:

retiring at least one remote key that was previously obtained via the allocate remote key verb with the consumer process employing a deallocate remote key verb.

16. (Previously Presented) The method of claim 1 wherein the remote key cannot be used to protect more than one memory region at a given instant.

17. (Previously Presented) The method of claim 1 further comprising:

reusing the remote key after the remote direct memory access operation from the second host processor endnode is completed.

18. (Previously Presented) The method of claim 1 further comprising:

disabling a translation for the remote key after the remote key is used for the remote direct memory access operation from the second host processor endnode.

19. (Previously Presented) A distributed computer system comprising:

communication fabric;

a first host processor endnode including:

a first processor;

a first memory configured to store a first consumer process which binds a remote key to a first address representing a contiguous memory address range accessible by the consumer process; and

a first network interface controller (NIC) sending the bound remote key and first address from the first host processor endnode on the communication fabric; and a second host processor endnode including:

a second processor;

a second (NIC) receiving the bound remote key and first address from the first host processor endnode via the communication fabric; and

a second memory configured to store a second consumer process performing a remote direct memory access operation from the second host processor endnode to access the contiguous memory address range including sending, via the second NIC, the bound remote key and the first address from the second host processor endnode to the first host processor endnode on the communication fabric.

20. (Previously Presented) The distributed computer system of claim 19 wherein the first memory is configured to store:

an operating system kernel process having a virtual memory manager controlling local memory access protection in the first host processor endnode.

21. (Previously Presented) The distributed computer system of claim 19 wherein in the remote direct memory operation if the bound remote key and corresponding first address supplied by the second host processor endnode do not match the bound remote key and first address in the first host processor endnode, the second host processor endnode is not granted access to the contiguous memory address range.

22. (Previously Presented) The distributed computer system of claim 19 wherein in the remote direct memory operation if the contiguous memory address range represented by the first address bound to the remote key supplied by the second host processor endnode is invalid, the second host processor endnode is not granted access to the contiguous memory address range.

23. (Previously Presented) The distributed computer system of claim 19 wherein the first address is an effective address pointing to an address space in memory accessible by the first consumer process.

24. (Previously Presented) The distributed computer system of claim 23 wherein the effective address points to a virtual address space.

25. (Previously Presented) The distributed computer system of claim 19 wherein the first consumer process is a user process.

26. (Previously Presented) The distributed computer system of claim 19 wherein the first consumer process is a kernel process.

27. (Previously Presented) The distributed computer system of claim 26 wherein the first address is a virtual address accessible by the first consumer process which is a consumer kernel process.

28. (Previously Presented) The distributed computer system of claim 19 wherein a consumer process employs a bind remote key verb to bind the first address to the remote key.

29. (Previously Presented) The distributed computer system of claim19 wherein a consumer process employs an allocate remote key verb to obtain at least one remote key.

30. (Previously Presented) The distributed computer system of claim19 wherein a consumer process employs an unbind remote key verb to unbind the remote key from the first address.

31. (Previously Presented) The distributed computer system of claim 29 wherein a consumer process employs a deallocate remote key verb to retire at least one remote key that was previously obtained via the allocate remote key verb.

32. (Previously Presented) The distributed computer system of claim19 wherein the remote key cannot be used to protect more than one memory region at a given instant.

33. (Previously Presented) The distributed computer system of claim19 wherein the first consumer process reuses the remote key after the remote direct memory access operation from the second host processor endnode is completed.

34. (Previously Presented) The distributed computer system of claim19 wherein the remote key is a one-shot validating mechanism such that a translation for the remote key is disabled after the remote key is used for the remote direct memory access operation from the second host processor endnode.

Appeal Brief to the Board of Patent Appeals and Interferences
Appellant: Michael R. Krause et al.
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EVIDENCE APPENDIX

None.

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RELATED PROCEEDINGS APPENDIX

None.